PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	**Shi-Tron LIN et al.**	Examiner:	Ori NADAV
Serial No.:	**09/779,096**	Art Unit:	2811
Filed:	February 8, 2001	Our Ref:	B-4104 618582-4
For:	"OUTPUT BUFFER WITH GOOD ESD PROTECTION"	Date:	December 14, 2004
		Re:	***Appeal to the Board of Appeals***

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection dated January 12, 2004, for the above identified patent application. The Notice of Appeal was filed on April 12, 2004. A Petition to Revive this application together with the requisite fee is submitted concurrently herewith. Enclosed please find a check in the amount of $500.00 for the fee set forth in 37 C.F.R. 1.17(c) for submitting this Brief. An Amendment After Final Rejection pursuant to 37 C.F.R. 1.116 is also submitted herewith. Entry of this Amendment prior to consideration of the present Brief is respectfully requested, because the Amendment solely cancels a number of the presently pending claims, thereby reducing the number of issues presented on appeal.

REAL PARTY IN INTEREST

The present application has been assigned to Winbond Electronics Corp. of Hsinchu, Taiwan.

STATUS OF CLAIMS

Claims 1-4, 14, 34, and 38-74 are pending in the Application and are reproduced in the accompanying appendix. Claims 2, 34, 38, 43-47 and 61-68 are the subject of this Appeal. Claims 1, 3-4, 14, 39-42, 48-60, and 69-74 are canceled by the Amendment After Final Rejection pursuant to 37 C.F.R. 1.116 submitted concurrently herewith, the entry of which is respectfully requested. The Examiner has withdrawn Claims 5-7, 11-12, 15-30, and 32-34 from consideration. Claim 8-10, 13, 31, and 35-37 have been previously canceled.

STATUS OF AMENDMENTS

An Amendment After Final Rejection is submitted concurrently herewith, the entry of which is respectfully requested pursuant to 37 C.F.R. 1.116.

SUMMARY OF THE INVENTION

The invention described and claimed in the present application relates to an output buffer that offers improved electrostatic discharge protection (specification, page 1, lines 8-9) and good voltage ringing and overshooting performance (p. 1, ll. 10-13). The output buffer employs two circuits, the so-called pull up circuit and pull down circuit (p. 6, ll. 30-32). The pull up circuit is coupled between a power line and a pad (p. 6, l. 33). The pull down circuit is coupled between another power line and the pad (p. 6, l. 34 – p. 7, l. 1). The pull down circuit includes a resistor , a capacitor, and an electrostatic discharge (ESD) protection component (p. 7, ll. 1-23). The resistor is comprised of a well region of a second conductivity type disposed on a substrate of a first conductivity type, and includes a first end and a second end (p. 7, ll. 2-5). The first end is a doped region of the second conductivity type at least partially overlapping the well region and is coupled to the pad (p. 7, ll. 5-8). A first doped region of the first conductivity type is also disposed within the well region (p. 7, ll. 9-11). The capacitor is coupled between the pad and the first doped region (p. 7, ll. 21-23). The ESD protection component is coupled between the second end of the resistor and the second power line (p. 7, ll. 11-19).

Under normal operating conditions, the first doped region is in an electrically floated state, the equivalent circuit of the pull down circuit thus consists of only the resistor and the ESD component, and the output buffer operates to suppress voltage ringing and overshooting, in the

manner of conventional output buffers. However, when an ESD occurs that is positive with reference to the power line, the first doped region is coupled to the first end of the resistor and the parasitic bipolar junction transistors (BJTs) that are created between the first doped region, the well region and the substrate, and between the well region, the substrate, and the source of the ESD protection component, respectively, are both triggered to release a large amount of ESD energy through a latch-up phenomenon (p. 8, ll. 10-25).

ISSUES

Issue 1: Whether Claim 34 is patentable under 35 U.S.C. 112.

Issue 2: Whether Claims 34, 44, 45 and 61-64 are patentable under 35 U.S.C. 102(b) over U.S. Patent No. 5,903,420 to Ham (hereinafter "Ham").

Issue 3: Whether Claims 34, 43, 45 and 61 are patentable under 35 U.S.C. 102(b) over U.S. Patent No. 5,343,053 to Avery (hereinafter "Avery").

Issue 4: Whether Claims 38, 46, 47 and 65-68 are patentable under 35 U.S.C. 102(b) over U.S. Patent No. 5,686,751 to Wu (hereinafter "Wu").

Issue 5: Whether Claim 34 is patentable under 35 U.S.C. 103(a) over Ham in view of the Applicants' Admitted Prior Art (hereinafter "AAPA").

Issue 6: Whether Claim 34 is patentable under 35 U.S.C. 103(a) over Avery in view of AAPA.

Issue 7: Whether Claim 2 is patentable under 35 U.S.C. 103(a) over Wu in view of AAPA.

GROUPING OF CLAIMS

For each ground of rejection which the Applicant contests herein and which applies to more than one claim, such additional claims, to the extent separately identified and argued below, do not stand or fall together.

THE ARGUMENT

Issue 1: Whether Claim 34 is patentable under 35 U.S.C. 112.

In section 4 of the Office Action of January 12, 2004, the Examiner rejects Claim 34 under 35 U.S.C. 112 as being indefinite. Specifically, the Examiner notes in section 5 that the limitations of "there is no DC connection between the doped region and the pad" as recited in claim 39, and of an electrically floated second doped region being coupled to a capacitor as recited in claim 60, are unclear. The Examiner makes no specific objection to the language of claim 34. Neither of the two phrases specifically identified by the Examiner are present in claim 34. Applicants thus submit that the Examiner has failed to make a proper rejection under 35 U.S.C. 112 and respectfully request that this rejection be overturned on appeal.

Issue 2: Whether Claims 34, 44, 45 and 61-64 are patentable under 35 U.S.C. 102(b) over U.S. Patent No. 5,903,420 to Ham (hereinafter "Ham").

In section 8 of the Office Action the Examiner rejects claims 34, 44, 45 and 61-64 as being anticipated by Ham. The Examiner asserts that Ham discloses all claimed limitations of claims 34 and 61, including that of a doped region of the first conductivity type electrically floated within a well region of a second conductivity type. This assertion is in error.

In the embodiments disclosed by Ham, N type region 46 is electrically coupled to the VDD through N-well 24 and N type region 52. In alternative embodiments, P type region 46 is electrically coupled to the VSS through P-well 22 and P type region 40. Clearly, the doped

region 46 in Ham is not electrically floated, regardless of its conductivity type. Because Ham does not teach, disclose or suggest an electrically floated doped region as recited in claims 34 and 61, and because claims 44 and 45 depend from claim 34 and claims 62-64 depend from claim 61, Applicants respectfully request that this rejection be overturned on appeal.

Issue 3: Whether Claims 34, 43, 45 and 61 are patentable under 35 U.S.C. 102(b) over U.S. Patent No. 5,343,053 to Avery (hereinafter "Avery").

In section 8 of the Office Action the Examiner further rejects claims 34, 43, 45 and 61 as being anticipated by Avery. The Examiner asserts that Avery discloses all claimed limitations of claims 34 and 61, including that of a first doped region 444 and a second doped region 438 of a second conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel region formed in between. Applicants submit that this assertion is incorrect.

In the embodiments of Avery, there is no gate on the substrate between the doped regions 444 and 438, such that no channel region as claimed can possibly be formed between these doped regions 444 and 438. Thus, Avery does not in fact teach, disclose or suggest "a first doped region and a second doped region of a second conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between" as recited by claims 34 and 61. Claims 43 and 45 depend from claim 34. In view of the preceding, Applicants respectfully request that this rejection be overturned on appeal.

Issue 4: Whether Claims 38, 46, 47 and 65-68 are patentable under 35 U.S.C. 102(b) over U.S. Patent No. 5,686,751 to Wu (hereinafter "Wu").

In section 8 of the Office Action the Examiner also rejects claims 38, 46, 47 and 65-68 as being anticipated by Wu. The Examiner asserts that Wu discloses all claimed limitations of claims 38 and 65, including that of a first doped region 214 and a second doped region 216 of the second conductive type formed in a substrate 200 of the first conductivity type. However, Wu in fact discloses that the first doped region 214 is N-type (col. 6, l. 1) whereas the second contact

regions 216 are P-type (col. 6, ll. 15-18). Furthermore, even if the Examiner intended to cite to second doped region 215, not 216, (and thus made a typographical error) Wu further teaches that the substrate 200 is also N-type, and thus the substrate of Wu is also of the second conductivity type, not the first conductivity type as per claims 38 and 65.

The Examiner further asserts that the resistor of Wu comprises a fourth doped region 224 and a fifth doped region 225 of the second conductive type formed in the well 220 of the second conductive type. However, as clearly disclosed by Wu (see, e.g., col. 6, ll. 23-31 and Fig.) the doped regions 224 and 225 are N-type and P-type, respectively, and thus are most definitely not both of the second conductive type, as recited in claims 38 and 65. however, are also not the same conductive type. Thus, Wu does not teach, disclose or suggest all limitations of claims 38 and 65. Claims 46 and 47 depend from claim 38, and claims 66-68 depend from claims 65. In view of the above, Applicants respectfully request that this rejection be overturned on appeal.

Issue 5: Whether Claim 34 is patentable under 35 U.S.C. 103(a) over Ham in view of the Applicants' Admitted Prior Art (hereinafter "AAPA").

In section 10 of the Office Action the Examiner finds claim 34 unpatentable under 35 U.S.C. 103(a) over Ham in view of AAPA. To establish a *prima facie* case of obviousness, the Examiner must show: (1) that there is some suggestion or motivation to modify the reference or to combine reference teachings; (2) that there is a reasonable expectation of success; and (3) that the prior art reference or references teach or suggest each and every claim limitation. See MPEP 2142. Further, the suggestion or motivation to modify or combine and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. The Applicant submits that the Examiner has neither adequately shown a motivation to combine the references in the manner done by the Examiner nor has the Examiner shown that the asserted combination teaches each and every element of the rejected claim. Therefore, the Applicant submits that the Examiner has not established a *prima facie* case of obviousness based on the cited prior art and/or AAPA, and the claim is in fact patentable over the art.

In the Action, the Examiner sets forth his reasons for rejecting claims 1, 31 and 39, but does not address claim 34 directly. Applicants have addressed Ham, as applied to claim 34, in

the previous discussion related to Issue 2. As discussed, in the embodiments disclosed by Ham, N type region 46 is electrically coupled to the VDD through N-well 24 and N type region 52. In alternative embodiments, P type region 46 is electrically coupled to the VSS through P-well 22 and P type region 40. Thus, the doped region 46 in Ham is not electrically floated, regardless of its conductivity type. There is also no teaching nor suggestion of an electrically floated doped region in AAPA. Therefore, because neither Ham nor AAPA teach, disclose or suggest an electrically floated doped region as recited in claim 34, Applicants respectfully request that this rejection be overturned on appeal.

Issue 6: Whether Claim 34 is patentable under 35 U.S.C. 103(a) over Avery in view of AAPA.

In section 11 of the Office Action the Examiner also finds claim 34 to be unpatentable under 35 U.S.C. 103(a) over Avery in view of AAPA, and avers that Avery discloses substantially the entire claimed structure "except using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad." Of course, this assertion runs directly contrary to the Examiner's rejection of the very same claim 34 under 102(b) in view of the very same Avery in section 8 of the Action, wherein the Examiner finds that Avery in fact discloses all limitations of claim 34 (page 5 of the Action, "Avery teaches in figure 9 and related text a second circuit coupled between a second power line 45 and the pad 47...").

Regardless, as explained above by Applicants in the discussion related to Issue 3, Avery does not in fact teach, disclose or suggest "a first doped region and a second doped region of a second conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between" as recited by claim 34, because the embodiments of Avery do not include a gate that would enable formation of such a channel region. Therefore, Avery fails to teach more than just using the device in an output buffer, as acknowledged by the Examiner, and because the Examiner has failed to make a *prima*

facie case of obviousness, Applicants respectfully request that this rejection be overturned on appeal.

Issue 7: Whether Claim 2 is patentable under 35 U.S.C. 103(a) over Wu in view of AAPA.

In section 11 of the Office Action the Examiner further finds claim 2 to be unpatentable under 35 U.S.C. 103(a) over Wu in view of AAPA, and once again opines that Wu discloses substantially the entire claimed structure "except using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad." The Examiner cites broadly to "figures 5 and 6 and related text" in support of his rejection, falling far short of his duty under MPEP 707.07(d) to state the grounds of rejection fully and clearly and avoid omnibus rejections. Nonetheless, Applicants have attempted to deduce the Examiner's actual reasoning in view of figures 5 and 6 and the related text of Wu and find that, regardless of the two possible readings of this reference, they are compelled to respectfully disagree with the Examiner.

Claim 2 recites, among others, a resistor constructed by a well region of a second conductivity type disposed on a substrate of a first conductivity type, the resistor comprising a first end being a doped region of the second conductivity type at least partially overlapping the well region and coupled to the pad, a first doped region of the first conductivity type disposed within the well region, and a capacitor coupled between the pad and the first doped region. Assuming that in the Examiner's reading of Wu, the resistor constructed by well region 220 has a first end (region 225), then the doped regions of the second conductivity type in the well region 220 are regions 225, and thus the two regions 225 correspond to the first end and the second end of Applicants' claim 2. However, the contact regions 225 of P+ type are connected to the node VSS because the contact regions 225 are bulk terminals of the second MOS transistor M7 (col. 6, ll. 29-31). Thus, regions 225 are not in fact coupled to the pad, and neither Wu nor AAPA teach a resistor with two ends of the second conductivity type as claimed.

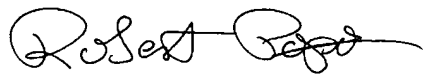
Alternatively, if the Examiner equates the resistor constructed by well region 210 with the claimed resistor, the doped regions of the first conductivity type in the well region 210 are

doped regions 214 and 215. The capacitor C2, however, is not coupled between the region 214 and the pad nor between the regions 215 and the pad. Thus, in Wu, there is no first doped region 30 of the first conductive type as claimed in claim 2. Therefore, Applicants submit that neither Wu nor AAPA teach a first doped region of the first conductive type as claimed, and because the Examiner has failed to make a *prima facie* case of obviousness, Applicants respectfully request that this rejection be overturned on appeal as well.

CONCLUSION

For the extensive reasons advanced above, Appellant respectfully contends that each claim is patentable. Therefore, reversal of all rejections and objections and re-opening of the prosecution is respectfully solicited.

Respectfully submitted,



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Attachments

Claims

1. An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

a resistor constructed by a well region of a second conductivity type disposed on a substrate of a first conductivity type, the resistor comprising a fourth doped region of the second conductivity type and a fifth doped region of the second conductivity type, the fourth doped region being coupled to the pad;

a first doped region of the first conductivity type, disposed within the well region, wherein the first doped region is electrically floated and spaced apart from the fourth doped region; and

an electrostatic discharge protection component, coupled between the fifth doped region and the second power line.

2. (previously presented) An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

a resistor constructed by a well region of a second

conductivity type disposed on a substrate of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region of the second conductivity type at least partially overlapping the well region and coupled to the pad;

a first doped region of the first conductivity type disposed within the well region;

a capacitor coupled between the pad and the first doped region; and

an electrostatic discharge protection component, coupled between the second end and the second power line.

3. The output buffer of claim 1, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the fifth doped region and the source being coupled to the second power line.

4. The output buffer of claim 3, wherein the drain is a second doped region of the second conductivity type and the source is a third doped region of the second conductivity type.

3-4. (cancelled)

5-7. (withdrawn)

8-10. (cancelled)

11-12. (withdrawn)

13. (cancelled)

14. The output buffer of claim 1, wherein the substrate is coupled to the second power line through the sixth doped region of the first conductivity type.

15-30. (withdrawn)

31. (cancelled)

32-33. (withdrawn)

34. (previously presented) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between;

a well region of the second conductivity type, formed in the substrate; and

a fourth doped region and a fifth doped region of the second conductivity type formed in the well region, the fourth

doped region coupled to the first node; and

a third doped region of the first conductivity type disposed within the well region, wherein the third doped region is electrically floated and is spaced apart from the fourth doped region, the first node is electrically coupled to the first doped region through the fourth doped region, the well region, and the fifth doped region, and the second node is electrically coupled to the second doped region.

35-37. (cancelled)

38. (previously presented) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel formed in between;

a resistor constructed by a well region of a second conductivity type being disposed on the substrate, the resistor comprising a fourth doped region and a fifth doped region of the second conductivity type; the fourth doped region coupled to the first node; and

a third doped region of the first conductivity type disposed within the well region, wherein the third doped region is coupled to the first node through a capacitor; the third doped region is spaced apart from the fourth doped region; the

first node is electrically coupled to the first doped region through the fourth doped region, the well region, and the fifth doped region; and the second node is electrically coupled to the second doped region.

39. An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a second doped region and a third doped region of a second conductivity type disposed in the well region. the second doped region being coupled to the pad:

a first doped region of the first conductivity type disposed within the well region, wherein there is no DC connection between the first doped region and the pad; and

an electrostatic discharge protection component coupled between the third doped region and the second power line.

40. The output buffer of claim 1, wherein the first doped region is electrically floating between the fourth doped region and the fifth doped region.

41. The output buffer of claim 1, wherein the first doped region is spaced apart from the fifth doped region.

42. The output buffer of claim 1, wherein the fifth doped region is at least partially overlapping with the well region.

43. The electrostatic discharge protection circuit of claim 34, wherein the third doped region is electrically floating between the fourth doped region and the fifth doped region.

44. The electrostatic discharge protection circuit of claim 34, wherein the third doped region is spaced apart from the fifth doped region.

45. The electrostatic discharge protection circuit of claim 34, wherein the fifth doped region is at least partially overlapping with the well region.

46. The electrostatic discharge protection circuit of claim 38, wherein the third doped region is disposed between the fourth doped region and the fifth doped region.

47. The electrostatic discharge protection circuit of claim 38, wherein the third doped region is spaced apart from the fifth doped region.

48. The output buffer of claim 39, wherein the first doped region is disposed between the second doped region and the third doped region.

49. The output buffer of claim 39, wherein the first doped region is spaced apart from the third doped region.

50. The output buffer of claim 39, wherein the first doped region is not directly connected to the pad.

51. The output buffer of claim 39, wherein the first doped region is not connected to the pad.

52. An output butter, comprising:

a first circuit coupled between a first power line and a pad; and a second circuit coupled between a second power line and the pad, the second circuit comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type disposed in the well region, the first doped region being coupled to the pad;

a third doped region of the first conductivity type disposed within the well region, wherein the third doped region is spaced apart from the first doped region, the first doped region is not electrically connected to the pad; and

an electrostatic discharge protection component coupled between the second doped region and the second power line.

53. A semiconductor device, comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region of the second conductivity type disposed in the well region and coupled to a pad; and

a second doped region of the first conductivity type disposed within the well region, wherein the second doped region is electrically floated and spaced apart from the first doped region; and

an electrostatic discharge protection component, coupled between the well region and a first power line.

54. The semiconductor device of claim 53, further comprising a third doped region of the second conductivity type disposed in the well region and coupled to the electrostatic discharge protection component.

55. The semiconductor device of claim 54, wherein the second doped region is electrically floating between the first doped region and the third doped region.

56. The semiconductor device of claim 54, wherein the second doped region is spaced apart from the third doped region.

57. The semiconductor device of claim 54, wherein the third doped region is at least partially overlapping with the well region.

58. The semiconductor device of claim 54, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the third doped region and the source being coupled to the first power line.

59. The semiconductor device of claim 54, wherein the drain is a fourth doped region of the second conductivity type, and the source is a fifth doped region of the second conductivity type.

60. A semiconductor device, comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region of the second conductivity type disposed in the well region and coupled to a pad;

a second doped region of the first conductivity type disposed within the well region, wherein the second doped region is electrically floated and spaced apart from the first doped region; and a capacitor coupled between the pad and the second doped region and an electrostatic discharge protection component, coupled between the well region and a first power line.

61. An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second

conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between;

a well region of the second conductivity type formed in the substrate;

a third doped region of the second conductivity type formed in the well region and coupled to the first node; and

a fourth doped region of the first conductivity type disposed within the well region, wherein the fourth doped region is electrically floated and is spaced apart from the third doped region, the first node is electrically coupled to the first doped region through the third doped region and well region; and, the second node is electrically coupled to the second doped region.

62. The electrostatic discharge protection circuit of claim 61, further comprising a fifth doped region of the second conductivity type disposed in the well region, wherein the fourth doped region is electrically floating between the third doped region and the fifth doped region.

63. The electrostatic discharge protection circuit of claim 62, wherein the fourth doped region is spaced apart from the fifth doped region.

64. The electrostatic discharge protection circuit of claim 62, wherein the fifth doped region is at least partially overlapping with the well region.

65. An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel formed in between;

a well region of the second conductivity type formed in the substrate; and

a third doped region of the second conductivity type disposed in the well region and coupled to the first node;

a fourth doped region of the first conductivity type disposed within the well region, wherein the fourth doped region is coupled to the first node through a capacitor; wherein

the fourth doped region is spaced apart from the third doped region; the first node is electrically coupled to the first doped region through the third doped region and the well region; and the second node is electrically coupled to the second doped region.

66. The electrostatic discharge protection circuit of claim 65, further comprising a fifth doped region of the second conductivity type disposed in the well region, and coupled to the second doped region.

67. The electrostatic discharge protection circuit of claim 65, wherein the fourth doped region is disposed between the third doped region and the fifth doped region.

68. The electrostatic discharge protection circuit of claim 65, wherein the fourth doped region is spaced apart from the fifth doped region.

69. A semiconductor device, comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region of a second conductivity type disposed in the well region and coupled to a pad;

a second doped region of the first conductivity type disposed within the well region, wherein the second doped region is electrically coupled to the pad without direct connectivity to the pad; and

an electrostatic discharge protection component coupled between the well region and a first power line.

70. The semiconductor device of claim 69, further comprising a third doped region of the second conductivity type disposed in the well region and coupled to the electrostatic discharge protection component.

71. The semiconductor device of claim 69, wherein the second doped region is disposed between the first doped region and the third doped region.

72. The semiconductor device of claim 69, wherein the second doped region is spaced apart from the third doped region.

73. The output buffer of claim 69, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the third doped region and the source being coupled to the first power line.

74. The semiconductor device of claim 69, wherein the drain is a fourth doped region of the second conductivity type, and the source is a fifth doped region of the second conductivity type.